

# **Notice of References Cited**

**Application/Control No.**

09/127,584

**Applicant(s)/Patent Under Reexamination**  
RAYNAUD ET AL.

**Examiner**

Douglas W. Sergeant

**Art Unit**

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## **U.S. PATENT DOCUMENTS**

*		DOCUMENT NO.	DATE	NAME	CLASS	SUBCLASS	DOCUMENT SOURCE **	
							APS	OTHER
<input type="checkbox"/>	A	US005870585A	Feb. 1999	Stapleton	395	500.36	<input type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/>	B	US005880971A	Mar. 1999	Dangelo et al.	395	500.07	<input type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/>	C	US005632032A	May. 1997	Ault et al.	709	100	<input type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/>	D	US005253255A	Oct. 1993	Carbine	714	734	<input type="checkbox"/>	<input type="checkbox"/>
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## **FOREIGN PATENT DOCUMENTS**

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUBCLASS	DOCUMENT SOURCE **	
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## **NON-PATENT DOCUMENTS**

*		DOCUMENT (Including Author, Title Date, Source, and Pertinent Pages)	DOCUMENT SOURCE **	
			APS	OTHER
<input type="checkbox"/>	U	Chen et al., "A Source-Level Dynamic Analysis Methodology and Tool for High-Level Synthesis", Proceedings of the Tenth International Symposium on System Synthesis, 1997, pp. 134 - 140, September 1997.	<input type="checkbox"/>	<input type="checkbox"/>
<input type="checkbox"/>	V	Kucukcakar et al., "Matisse: An Architectural Design Tool for Commodity IC's", IEEE Design & Test of Computers, Vol. 15, Issue 2, pp. 22 - 33, June 1998.	<input type="checkbox"/>	<input type="checkbox"/>
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<input type="checkbox"/>	X	Fang et al., "A Real-Time RTL Engineering-Change Method Supporting On-Line Debugging for Logic-Emulation Applications", Proceedings of the 34th Design Automation Conference, pp. 101-106, June 1997.	<input type="checkbox"/>	<input type="checkbox"/>

\*A copy of this reference is not being furnished with this Office action. (See Manual of Patent Examining Procedure, Section 707.05(a).)

\*\*APS encompasses any electronic search i.e. text, image, and Commercial Databases.

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PTO-892 (Rev. 03-98)

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Part of Paper No. 5